VDMOS Parameter Extraction
Part 1 – The quick method using datasheets

What we need for simulating power amplifiers is a simple non-physical model [footnote 1] like the Level 1 model [**Ref 1**] with a minimum number of parameters such as Vth, Kp, Lambda, Rs, Rd, Cgs, Cgd that define the underlying first-order effects plus subthreshold conduction.

The default MOSFET model for LTspice is the VDMOS [**Ref 2**, **Ref 3**]. It is a proprietary model overseen by Mike Engelhardt of Linear Technology, and the main DC equations are the Shickman Hodges Level 1 MOSFET model. December 2014 Mike added subthreshold conduction to the VDMOS which means the VDMOS model is now good for simulating Class-AB amplifiers [**Ref 4**].

Parameters for the VDMOS can be extracted from datasheet plots. There are a few rules of thumb that can yield quick and still useful simulations. A better fit can be obtained by manually iterating these initial values. To avoid frustration due to the interaction of several parameters it is helpful to know the best order of parameters to follow.

If you are just after a **quick way** to extract the VDMOS parameters then this Part 1 is all that you need. Bob Cordell's "Power Amplifier Design" 2nd Edition has Chapter 23 on getting started using LTspice and Chapter 24 on extracting parameters for BJT's [**Ref 5** Bob's site]. This paper fills in a few gaps for extracting parameters for the VDMOS model since there is not much available on the web.

Part 2 covers a new approach that can find the two most difficult parameters Kp and Vth accurately without iterations. The other DC parameters follow relatively easily. My new approach uses the derivative of √Id versus Vgs to extract Kp and Vth. The derivative of √Id versus Vgs also allows the subthreshold parameter to be conveniently found using moderate inversion currents rather than very low weak inversion currents which are difficult to measure due to the body diodes reverse current in power MOSFET's. To check my new approach, I measured the Exicon lateral 20N20 and 20P20 pair and 10N20 and 10P20 pair as accurately as I could using a home-made pulse tester with temperature control for 25C and 75C measurements. The pulse jig circuit and measurement procedure is covered in a separate document [**Ref 8**].

Having extracted the lateral MOSFET's parameters for the VDMOS, I then used the VDMOS model to generate Class-AB crossover 'wingspread' gain curves. These simulated curves were compared to measured lateral MOSFET's 'wingspread' curves using an Audio Precision tester from another source [**Ref 9**]. My simulated VDMOS 'wingspread' curves were found to be very close to the measured plots. This is shown at the end of Part 2 in Figure 11.

Also I fitted my data to the EKV model and plotted them together with the measure AP 'wingspread' plots the EKV fit was very close to the measured plots also. So the VDMOS DC model was found to be just as good as the EKV DC model for the purpose of generating realistic 'wingspread' plots for power amplifier simulations. The VDMOS includes several useful parameters (Lambda and Mtriode) for power amplifier simulations that the EKV does not have so the VDMOS is therefore preferred over the EKV model.

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1 Most MOSFET models are physical models as used by foundries to manufacture MOSFET's involving Length, Width and many other physical measurements. But for bought MOSFET's we want parameters that can be obtained from datasheet plots or bench measurements; physical models are a pain to use because we can't work backwards to get the physical parameters. What we need is a simplistic non-physical model like the Level 1 model with minimal parameters such as Vth, Kp, Lambda, Rs, Rd, Cgs, Cgd and the body diode to define the first order effects.

The VDMOS model parameters

There are many MOSFET's in the LTspice MOSFET library all with subthreshold conduction (since January 2017). Temperature coefficients were added to the VDMOS model May 2019 [ref Help]. But the standard library has not yet been updated to use these temperature coefficients (as of July 2019). Library models do have fixed temp co's, like Bex=-1.5 for Kp, Vtotc=-1mV/°C, but are invariably too low for typical power MOSFET's.

This document has been updated (July 209) for extracting the new temperature coefficients for the VDMOS which includes the body diode.
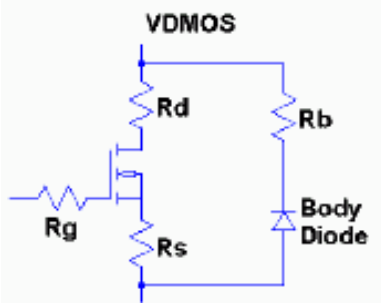
Illustration 1:
VDMOS + body diode
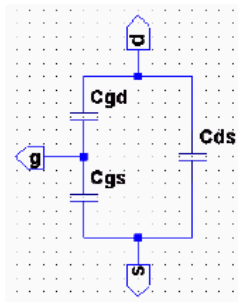
Illustration 2:
MOSFET caps
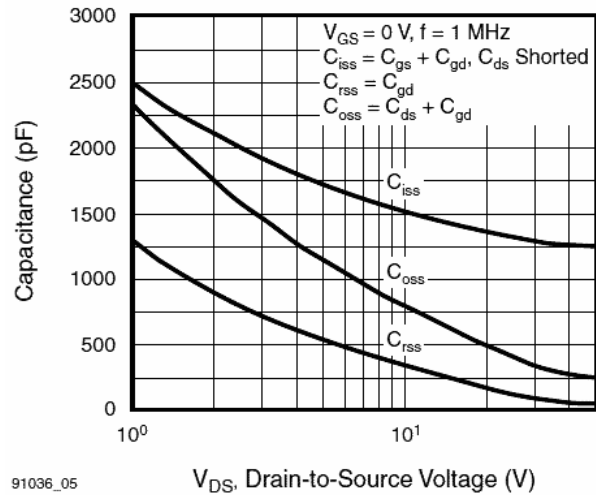
Illustration 3: IRFP240 Vishay

Illustration 1 shows the VDMOS and the body diode components.

Illustration 2 shows the internal MOS capacitors with the MOSFET. These capacitors are with NO MOSFET current (Vgs=0). In the VDMOS Cgs is approximated as a fixed value. Cgs can't be measured directly due to the other capacitances; Cgs can be found by solving simultaneous equations from measured Ciss, Crss and Coss which are given in datasheets, e.g. **Illustration 3** from Vishay IRFP240 datasheet. Notice Cgd is easy because it is Crss on datasheets.

Because both Cgd and Cds are nonlinear capacitors with Vds (**Illustration 3**) both Cgd and Cds require a special capacitance model inside the VDMOS model [ref Help]. The VDMOS uses parameters Cgdmax and Cgdmin and swing parameter 'a' for Cgd (same as Crss in the plots). The source-drain capacitance is modelled by the graded capacitance of the body diode across the source-drain (as shown above with body diode resistance Rb in series with this diode).

Equations can be used to convert from Ciss, Crss and Coss to Cgs, Cgd and Cds in the example below courtesy Hendrik Zwerver [3]. I have found you don't need to use any maths if you guess ball-park values and put them into a plotter jig that shows capacitance directly so you can iterate easily to get the same plots as the datasheet. Several jigs available for download at my site [11].

Part 1: Using equations to estimate VDMOS parameters from datasheets

This first example below uses datasheet values and equations to get an idea of where to get values and how good these first-time-around values are compared to a finalized model. I chose the IRFP240 because it is in the LTspice standard library.

Table 1: Extracting parameters using Hendrik Jan Zwerver's equations [**Ref 3**]

#	VDMOS parameter	Look for these values on the datasheet
1	Kp Transconductance parameter	= Gfs [*ignore units, typ. Gfs given at ~½ IDcont@25°C]

#	VDMOS parameter	Formula/Value
2	Vto Threshold voltage (at Tamb 25°C)	= Vgs(th) [*assume middle value of max/min range]
3	Rs	= (Vgsmax –√(2*Idmax/Gfs) – Vto)/Idmax
4	Rd	= Rdson – Rs – 1/[Gfs(10 – Rs/Rdson – Vto)]
5	Ksubthres	= 0.1 [default]
6	Cgdmax	=Crssmax+(Crssmax-Crssmin)/ATAN(10000)
7	Cdgmin	=Crssmin
8	A (nonlinear Cgd slope factor at Vds=0)	Range=0.2–2.5, Typical=0.3, Default=1
9	Cgs (assumed constant in the VDMOS)	=Ciss – Crss
10	Cjo body diode Cds @ Vds=0	=(Cossmax-Crssmax*Cgs/(Crssmax+Cgs))
11	M Body diode grading coefficient (Default=0.5)	=-LOG(Cds_{25V}/Cjo)/LOG(1+25/0.75)
12	Vj Body diode junction potential (Default=1)	"To be sure set Vj=0.75" [says Hendrik]
13	Rg Gate ohmic resistance	=Rg [*not often quoted, try Rg ≈ f-3dB/(2*pi*Cgs), else Rg ≈ Ton/(2.2*Ciss) – RgJig]
14	Rb	=Vd/Id –N*Vt/Id*Ln(Id/Is +1) Vt=KT/q=26mV 27°C
15	Is	try Idss [*body diode]
16	N	[*body diode n-ch typ. N=1-2, p-ch typ N=2-6]
17	Pchan	Specify for P-channel within the .model (...) brackets
18	Rds (optional)	[*not normally needed – only add if simulation convergence fails, eg add Rds=1e7 for a 10A MOSFET]
19	Ron (optional)	[manufactures value]
20	Qg (optional)	Qg [max total gate charge Vgs=10V, IDcont]]
21	Vds (optional)	[manufactures absolute Vmax]
22	Mfg (recommended)	=VishMe1907dd [your model date code,eg, YYMMDD]

* My comments added.

Step 1: Using Hendrik's estimates for the IRFP240

I'm using the 9 May 2012 datasheet.

Table 2: Hendrik's approach for the Vishay IRFP240

#	VDMOS parameter for IRFP240	Datasheet (start at 25C)
1	Kp	= 6.5
2	Vto	= 3
3	Rs	=(10-√(2*60/6.5)-3)/60 = 45m
4	Rd	= 0.18-0.045-1/[6.5(10-45m/180m-3)]=112m
5	Ksubthres	Use 0.1 [default]
6	Cgdmax	=Crssmax+(Crssmax-Crssmin)/ATAN(10000)=1.3n

7	Cdgmin	= Crssmin = 25p
8	'a' (nonlinear Cgd slope factor at Vds=0)	Typical 0.3 defaults to 1.0
9	Cgs	=Ciss-Crss = 2500p-1300p = 1.2n
10	Cjo	=(Cossmax-Crssmax*Cgs/(Crssmax+Cgs)) = 2400p – 624p = 1780p
11	M	=-LOG(Cds_{25v}/Cjo)/LOG(1+25/0.75) = – Log(287p/1780p)/1.536 = 0.52
12	Vj=0.75	To be sure set Vj to 0.75 [says Hendrik]
13	Rg	Rg≈Ton/(2.2*Ciss)-RgJig=51ns/(2.2*1.3nF)–9.1= 9R
14	Rb	=Vd/Id – N*Vt/Id*Ln(Id/Is+1) = 1.5/60 – 0.026/60*Ln(60/25u) = 19m
15	Is	= 25u
16	N=1.5	= 1.5 [body diode n-ch typ. N=1-2, p-ch typ N=2-6]
17	pchan	Don't specify (only if p-chan)
18	Rds	= 0.18
19	Vds	= 200 [datasheet absolute Vmax]
20	Ron	= 180m
21	Qg	= 45nC [Vgs=10V, Id=18A]
22	Mfg	=VishMe1907dd
23	Lambda*	=1/V_A where V_A is the Early voltage (x-axis intercept)

*Lambda was not included by Hendrik. A quick method uses the inverse of the Early voltage from x-axis intercept.

Summary for the 'Quick' IRFP240 using Hendrik's approach is below:

	Vto	Kp	Lambda	Rs	Rd	Ksub	Cgd max	Cgd min	a	Cgs	Cjo	M	N	Rb
Quick-v1	3 / 4†	6.5	0*	45m	112m	0.1	1.3n	25p	1*	1.2n	1.8n	0.52	1	19m
Final	4	6	3m	40m	150m	0.15	1.34n	10p	1*	1.2n	1.n	0.4*	1.5	10m

* unspecified parameters take the default values see LTspice Help file >F1>'M' for MOSFET > scroll down to VDMOS.
† See text. We are free to choose Vto anywhere in the Max to Min range.

The actual model listing is below:

```
*VDMOS with subthreshold (c) Ian Hegglun for 25C
.model IRFP240-v1 VDMOS (Rg=9 Vto=4 Kp=6.5 Rs=45m Rd=112m Ksubthres=0.1
+ Cgdmax=1.3n Cgdmin=25p Cgs=1.2n Cjo=1.8n m=0.52 VJ=0.75 IS=25u N=1.5 Rb=19m
Vds=200 Ron=0.18 Qg=45nC mfg=IH1907)
```

Next I use a plot jig to compare the two models. It can be downloaded **Ref 11**. How to use Appendix 1.

To compare the Quick model with the Final model (below) and I change the Vto of the Quick model to match my Final model which is 4V. The Vto varies so much from batch to batch so anything in the Max to Min range can be used, in this case anything in the range of 2-4V will do. My Final model has Vto=4 and that was to match the LTspice IRFP240 internal model and 4V matches to the Cordell IRFP240C model. If you want to get the Vto to match a batch of IRFP240's that you have then take a sample and use the mean Vto for your simulations.

My Final model is given below with comparison plots:

```
*VDMOS with subthreshold (c) Ian Hegglun
.model IRFP240h VDMOS (Rg=17 Vto=4.0 Kp=6 Lambda=3m
+ Rs=40m Ksubthres=0.15 Mtriode=0.35 Rd=0.15
+ Bex=-2.3 Vtotc=-6m Tksubthres1=4m Trs1=3.5m Trd1=5m
+ Cgdmax=1.3n Cgdmin=10p a=0.35 Cgs=1.2n Cjo=1n
+ m=0.4 VJ=0.75 IS=10n N=1.5 Eg=1.5 Rb=10m Trb1=2.5m
+ Vds=200 Ron=0.15 Qg=45nC mfg=VishIH1907)
```
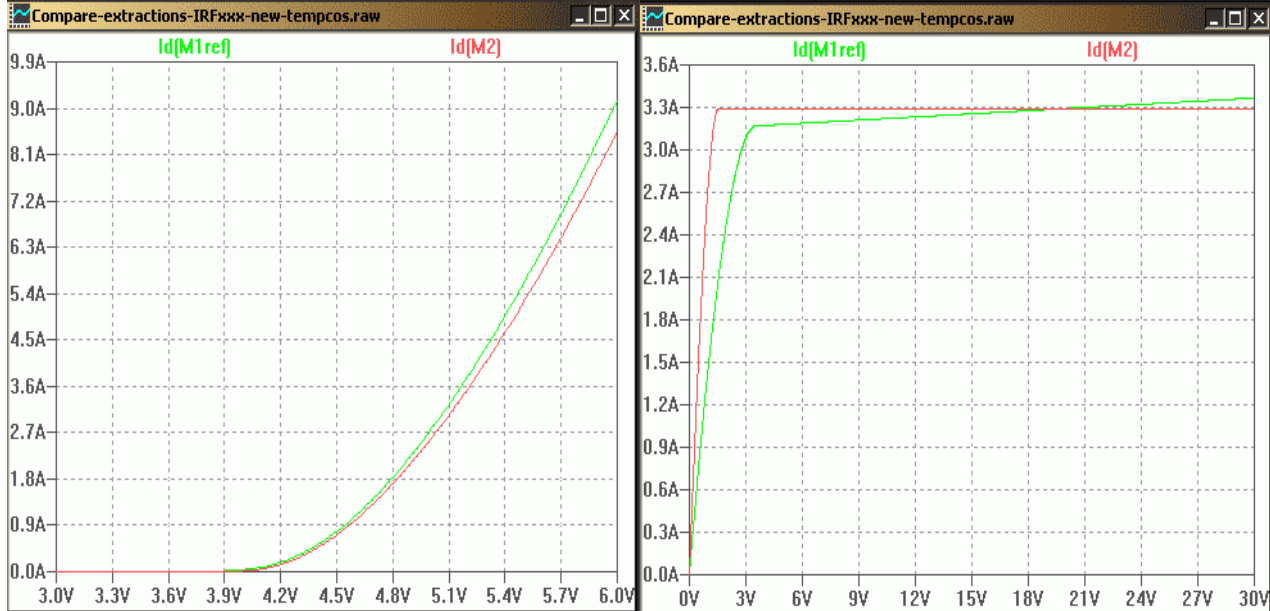

Id vs Vgs (L) and Id vs Vds (R). Two IRFP240 models Red = Quick-v1, Green = Final

Our Quick-v1 model using Hendrik's approach looks pretty darn good, don't you think?

Now some tweaking to get the drain conductance better – by adding parameter Lambda.

Step 2: Tweaking the VDMOS parameters

Choosing a rough value for Lambda is required for the **Id vs Vds plot slope**. Lambda affects the Id vs Vgs plot at high currents. A quick method to find Lambda is to use the inverse of the Early voltage from x-axis intercept.

The IRFP240 datasheet Figure 1 **Id vs Vds plot slope** is positive only for Vgs=4.5V and 5.0V but higher than this the slope turns negative which is caused by self heating, so the higher ones cannot be used for finding Lambda.

For the 5.0V plot the current rises from 2.5A to 2.8A for Vds of 20V to 50V.

Slope = 300mA/30V = 0.01 A/V, then use

Lambda = Slope/Id=10m/2.5 = 4m V^{-1}

The model listing for Quick-v2 becomes:

```
*VDMOS with subthreshold (c) Ian Hegglun for 25C
.model IRFP240-v2 VDMOS (Rg=9 Vto=4.0 Kp=6.5 Lambda=4m Rs=45m Rd=112m
Ksubthres=0.1 Cgdmax=1.3n Cgdmin=25p Cgs=1.2n Cjo=1.8n m=0.52 VJ=0.75 IS=25u
N=1.5Rb=19m Vds=200 Ron=0.18 Qg=45nC mfg=IHKT1907)
```

The new plot are shown below. Red = Quick-v2, Green = Final model, Tj is 25°C.
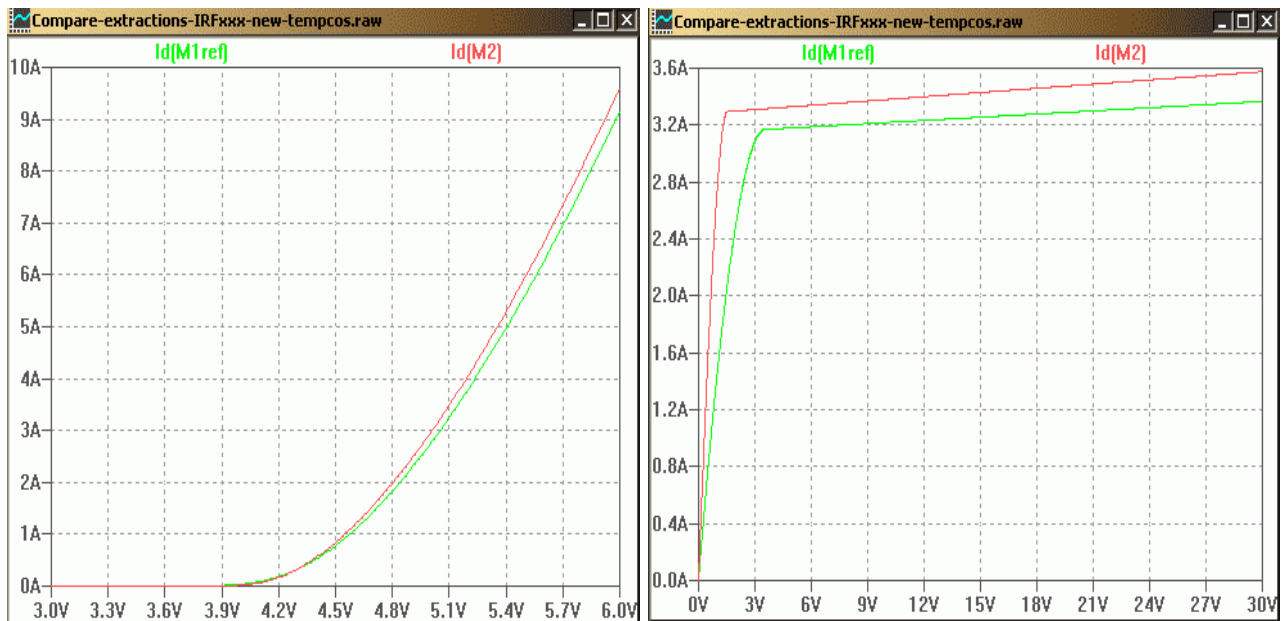
Id vs Vgs (L) and Id vs Vds (R). Two IRFP240 models Red = Quick-v2, Green = Final

We now have some slope in the Id vs. Vgs plot. This is probably good enough for 25°C.

Next add Temp Co's for Vto and Kp to look like the 150°C plot (datasheet Figure's 2, 3).

Tweaking the Temp Co's

The plot below is the same as above (Quick-v2) but now with Temp stepped 25°C and 150°C (as per the datasheet).
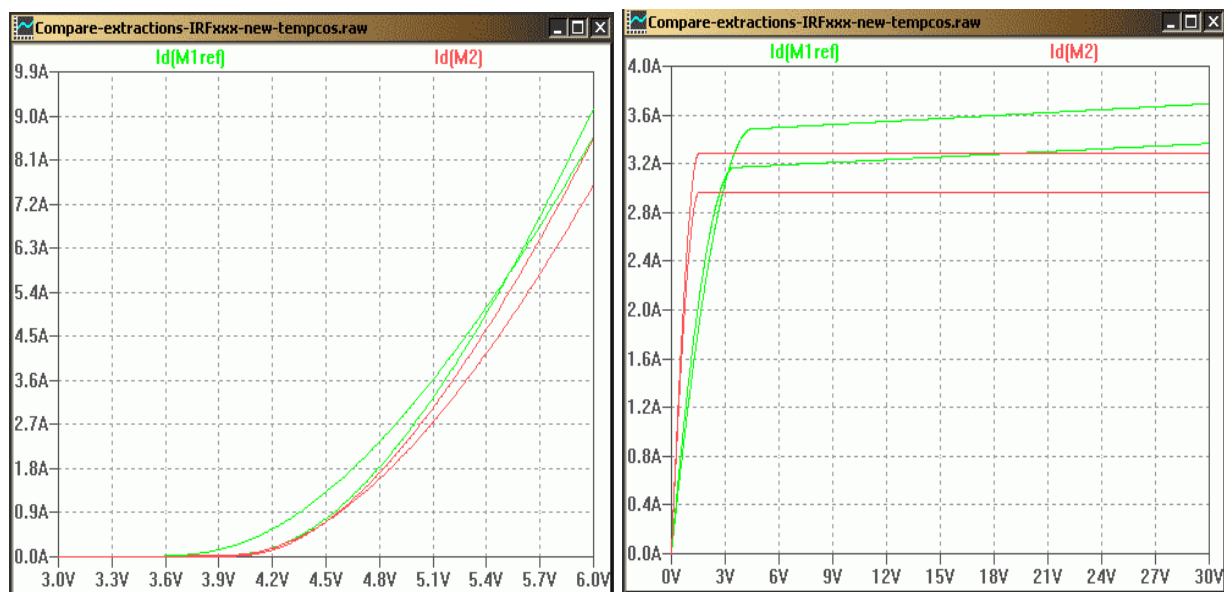
Id vs Vgs (L) and Id vs Vds (R), Step Tj 25°& 150°C. Red = Quick-v2, Green = Final

The temp. co. for Vto is VtoTc and for Kp is called Bex (Beta exponent where Beta is an alternative name for Kp).

The default VtoTc is -1mV/°C for n-channel (+1mV/°C for p-channel). Typically power MOSFET's are in the 3mV/°C to 10mV/°C range. The default Bex is -1.5 and typically power MOSFET's are in the -2 to -2.5 range.

We can choose mid-range values VtoTc = - 5mV/°C and Bex=-2.2 and see how that looks. See the

plots below.

```
*VDMOS with subthreshold (c) Ian Hegglun fitted to 25C and 150C
.model IRFP240-v3 VDMOS (Rg=9 Vto=4.0 Vtotc=-5m Kp=6.5 Bex=-2.2 Lambda=4m Rs=45m
Rd=112m Ksubthres=0.1 Cgdmax=1.3n Cgdmin=25p Cgs=1.2n Cjo=1.8n m=0.52 VJ=0.75
IS=25u N=1.5 Rb=19m Vds=200 Ron=0.18 Qg=45nC mfg=IHKT1907)
```
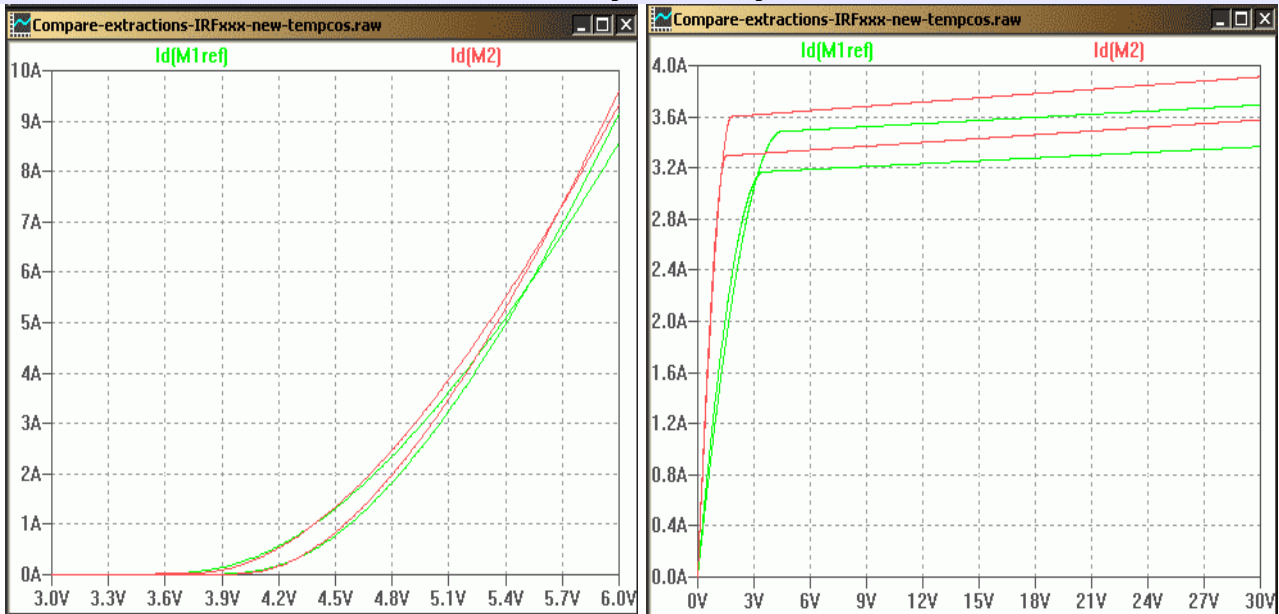

Id vs Vgs (L) and Id vs Vds (R), Step Tj 25°& 150°C. Red = Quick-v3, Green = Final

The new Id vs. Vgs plot now tracks good enough with temperature.

The initial slope of the **Id vs Vds** plot (near the origin) could be improved to match the datasheet plot by increasing Rd. Once the initial slope is about right then reduce Mtriode to get to turn around at the top to match the datasheets turn around. Increase Rd to 150m and then **Mtriode to 0.3** and we get the plots below.

```
*VDMOS with subthreshold (c) Ian Hegglun fitted to 25C and 150C
.model IRFP240-v4 VDMOS (Rg=9 Vto=4.0 Vtotc=-5m Kp=6.5 Bex=-2.2 Lambda=4m Rs=45m
Rd=140m Ksubthres=0.1 Mtriode=0.3 Cgdmax=1.3n Cgdmin=25p Cgs=1.2n Cjo=1.8n
m=0.52 VJ=0.75 IS=25u N=1.5 Rb=19m Vds=200 Ron=0.18 Qg=45nC mfg=IHKT1907)
```
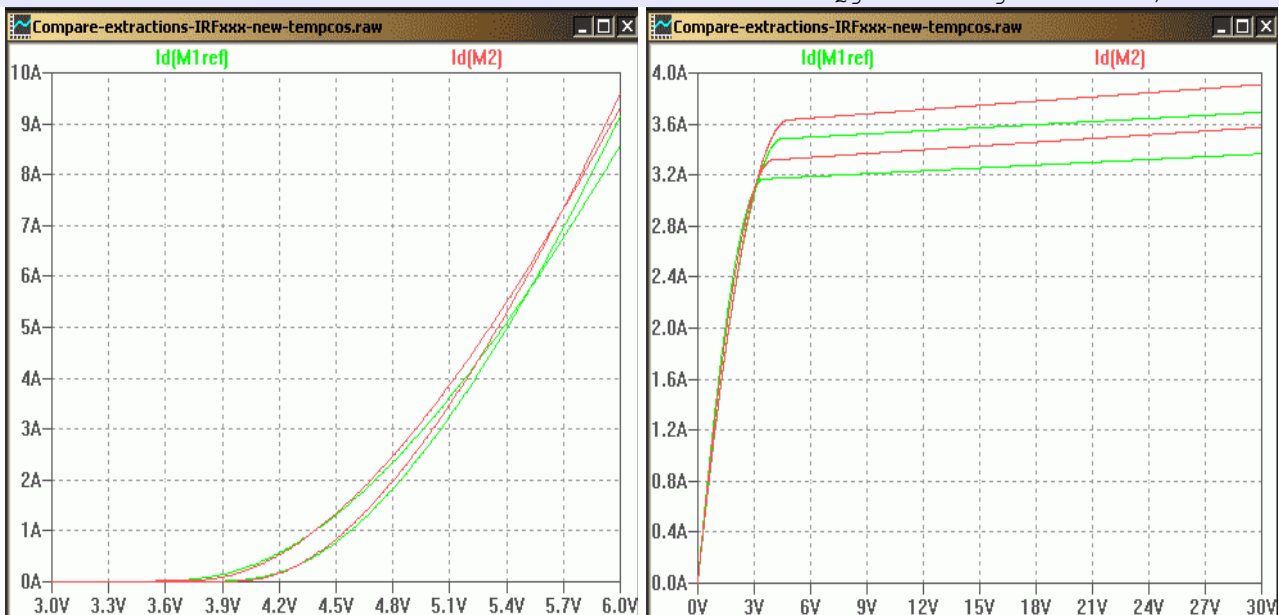

Id vs Vgs (L) and Id vs Vds (R), Step Tj 25°& 150°C. Red = Quick-v4, Green = Final

The new Id vs. Vds plot now looks good enough. We are about done for the DC parameters. The AC parameters are next then the body diode.

But before doing the AC parameters you may like to compare the Quick-v4 plots with the model already in LTspice:

```
.model IRFP240 VDMOS(Rg=3 Vto=4 Rd=72m Rs=18m Rb=36m Kp=4.9 Lambda=0.03
Cgdmax=1.34n Cgdmin=0.1n Cgs=1.25n Cjo=1.25n Is=67p ksubthres=0.1
mfg=International_Rectifier Vds=200 Ron=180m Qg=70n)
```

Note: This model uses default temperature coefficients Bex=-1.5 and Vto has -1mV/°C (for n-ch).
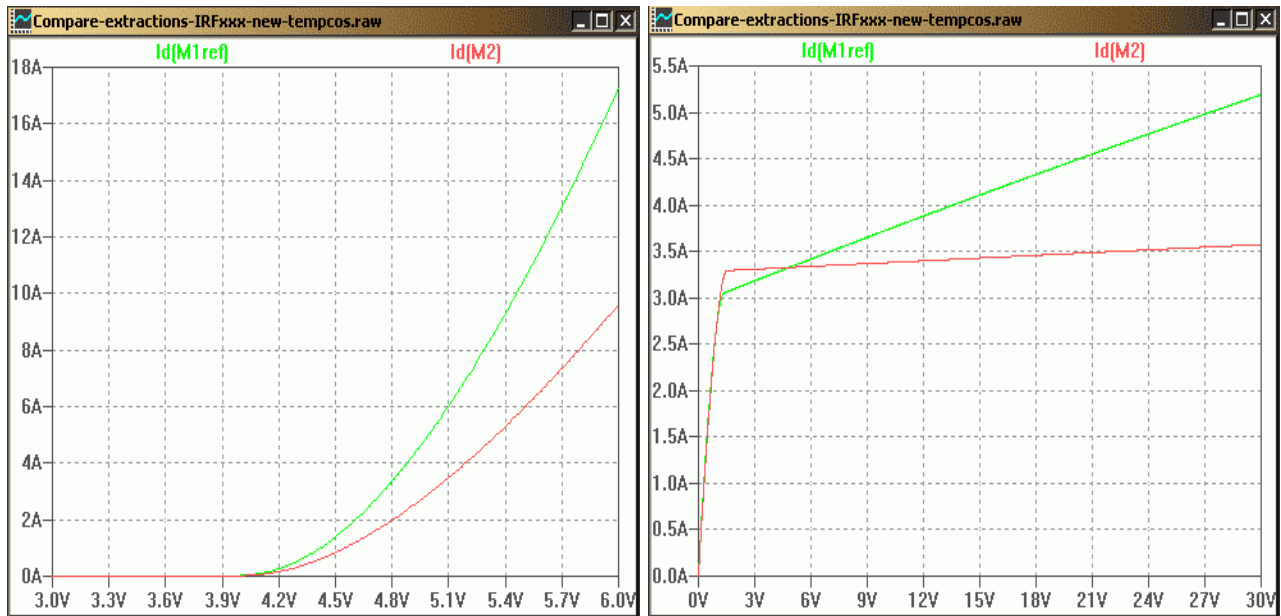
Id vs Vgs (L) and Id vs Vds (R). Red = Quick-v4, Green = Lt-internal lib.

The huge difference could be due to using a different datasheet since the IRFP240 was once available for two different manufacturers with different process settings.

Getting LTspice to generate curves from datasheets ?

In the above graphs you can easily see how close your Quick models is to my Final model. This is useful for this tutorial. But usually you can't do this. Wouldn't it be nice if we could get LTspice to generate curves from datasheets? Well, it can be done. But it takes about 30 minutes per curve and you want 2 curves (one Id vs Vgs and one Id vs Vds) and this makes getting a Quick model done twice as long. Appendix 5 explains how to use the free Graph Grabber software.

Tweaking the gate charge

There are two jigs, one for plotting gate charge (Gate voltage vs Gate charge) and another to plot Drain capacitance vs Vds. Start with a=0.3.

First the jig to plot Gate charge [**Ref 11**] to check IRFP240 datasheet plot Figure 6.

Parameters Cgs, Cgdmax and Cgdmin and Cjo can be obtained from IRFP240 datasheet plot Figure 5 which is annotated below.
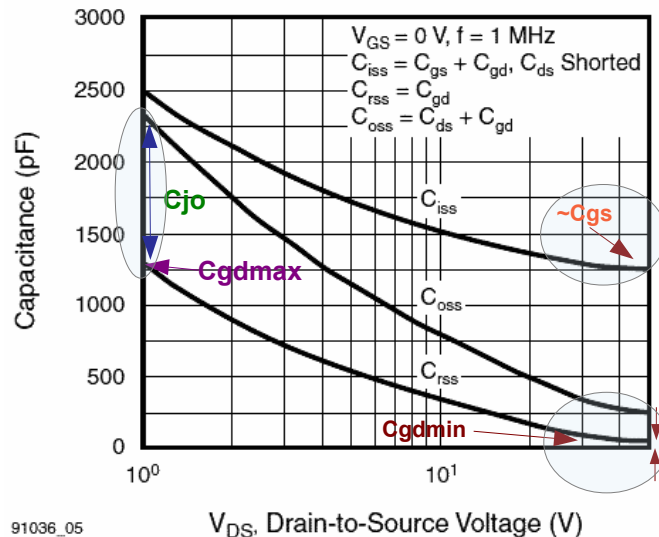
Illustration 4: IRFP240 Typical Capacitance vs. Drain-to-Source Voltage (DS Fig. 5)

You should have a go at using this jig to step Cgs, eg,

```
.Step param Cgs List 500p 1000p 1500p
```

Stepping Cgs shows the start *ramp slope* falls with higher Cgs. For the IRFP240 the Cgs was already correct at 1,2nF.

You can see what effect each parameter has by enabling stepping one parameter at a time, eg,

```
.Step param Cgdmax List 1n 2n 3n
```
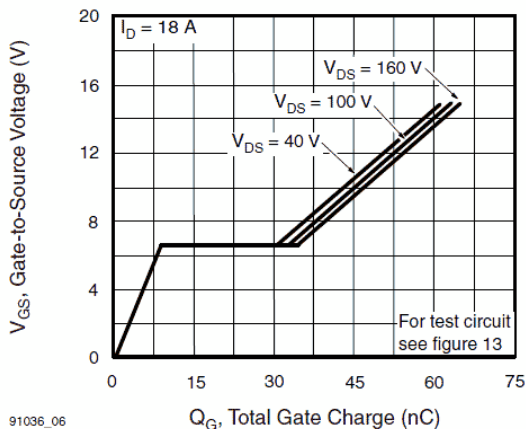

Illustration 5. IRFP240 DS Fig.6 Datasheet Gate charge plot
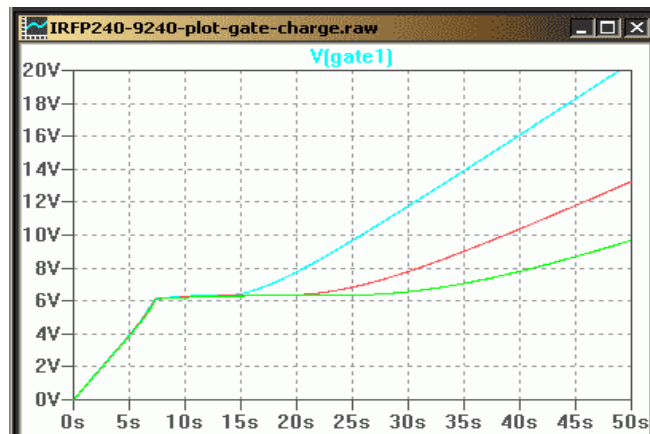
Illustration 6. Quick-v4 model (Blue & Red) with Cgdmax stepped 1n, 2n, 3n, Vds=100V.

Stepping Cgdmax causes the top end slope to decrease as well as shift the break-point from the plateau region (using an idealised intersection of straight lines like the datasheet plots). Therefore choose Cgdmax to get the slope of the datasheet top-end.

The already chosen value for **Cgdmax of 1.3nF** is near enough; notice it is the same as in the datasheet Fig.5. Using Cgdmax from Fig.5 is not always the best value. Use the jig to check the slope and intersection with the plateau. Sometimes you can't find a value that agrees with both Fig.5 and Fig.6 in which case I split the error over the 3 capacitances (Cgdmax, Cgdmin and Cgs).

Cgdmax and Cgdmin values are needed for power amplifier simulations because they introduce high frequency distortion and affect the compensation for clean clip recovery. It is not so important to get accurate values for the model as long as the maximum and minimum Cgd values do vary with

Vds – which is why we need the VDMOS model. Most power MOSFET models from manufacturers to not model this effect at all!

Next Cgdmin. This is Crss limit at high Vds from the IRFP240 datasheet (Figure 5 Capacitance vs. Drain-to-Source Voltage). It's about 10pF at the limit of the graph which ends at 50V. It might still go lower but use 10pF for now. Run the jig stepping Cgdmin over say 5p, 10p and 20p to see how these values affect the total gate charge plots. Cgdmin changes the spacing when Vds is stepped without changing the slope.
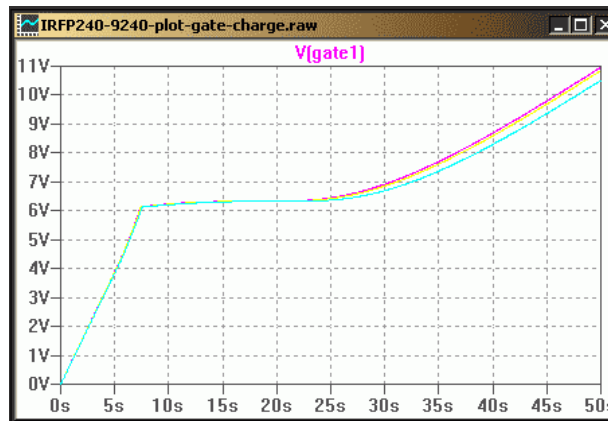
Illustration 7: IRFP240 Gdgmin stepped 5p, 10p,20p

Parameter 'a' is then chosen to shift the break point (idealised intersection using straight lines) from the plateau region. Start with a=0.3. Increasing 'a' shifts the break point to the left. We will use **Cgdmin=10pF and a=0.3**.

Parameter Cjo is for the body diode. Cjo is added to the MOSFET's intrinsic Cds giving total Cds. We only need find a value for Cjo (not Cds) and this is done in the next section for the body diode.

> BTW if you are interested in how this jig works – it injects a current ramp of 1nA <u>per second</u> into the gate while a drain current of 18A is forced through the drain (as per the datasheet test) and the drain-source voltage is pulled down as a result of the gate voltage changing. There is Miller feedback which is what causes the plateau region. Plotting Vgs against time gives the x-axis units of nano-Coulombs (nC) since gate current is *nA per second* and *Q= Current × time*.

Tweaking the body diode capacitance

Cjo is the diode junction capacitance at Vds=<u>0</u>. It is extracted using another jig for plotting total Cds versus Vds which is the same thing as plotting Coss vs. Vds **[Ref 11]**.

The Cds plot also allows the M parameter for the body diode capacitance, where M changes the rate of fall off of Cds/Coss with Vds.

The first parameter is Cjo. This can usually be got from the Capacitance vs. Drain-to-Source Voltage (IRFP240 datasheet Fig.5). Cjo = 2400pF – 1250pF = 1150pF. Hendrik's calculation above gave 1800pF but it seems using Fig.5 method get's the initial value for Cjo closer. A rounded value of 1000pF (**Cjo=1n**) will be used for the -v5 model below.

You could step Cjo in the jig but it doesn't help much. Try

```
.Step param Cjo List 2n 1.5n 1n
```

Next the parameter 'M' using the jig
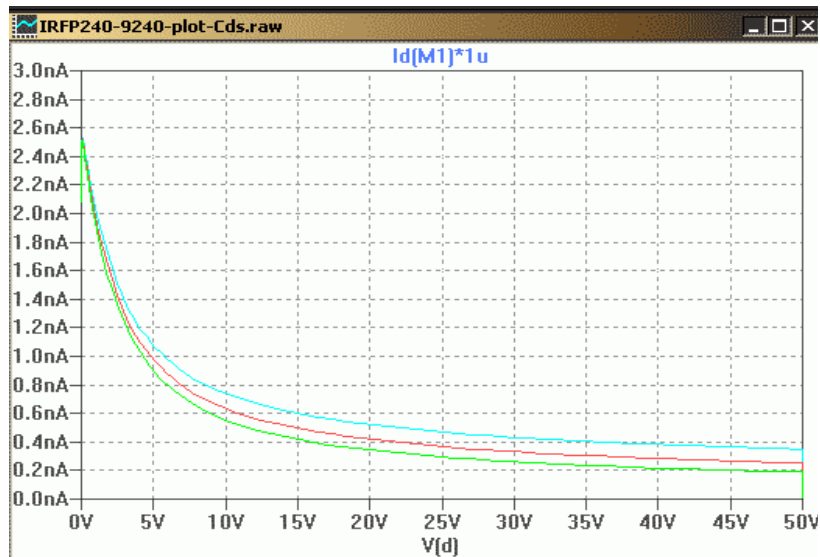
```
.Step param 'M' List 0.3 0.4 0.5
```

Illustration 8: IRFP240 body diode 'M' stepped 0.3, 0.4, 0.5

Probing Cds at Vds=50V is about right with M=0.4.

> BTW if you are interested in how this jig works – this jig forces a *ramp voltage* across the drain-source with the gate voltage set to zero, and the drain current is plotted against Vds. With a voltage ramp of 100 volts in 100us we get 1A and so we <u>scale the Id plot by a factor of 1n</u> to read the current as <u>nano</u> Farads. (This only works for 100V in 100us so don't change just the voltage to reset the plot range, but scale <u>both</u> Vpk and sweep time together, eg, 50V in 50us).

Next, parameter 'a'. It determines the slope of Cds decrease as Vds increases due to Cgdmax. It is fitted using the Cds vs. Vds plot jig <u>after</u> Cjo, Vj and M have been chosen. Fit 'a' using the Cds value when Vds=10V as found from the Capacitance vs. Drain-to-Source Voltage (IRFP240 datasheet Fig.5).
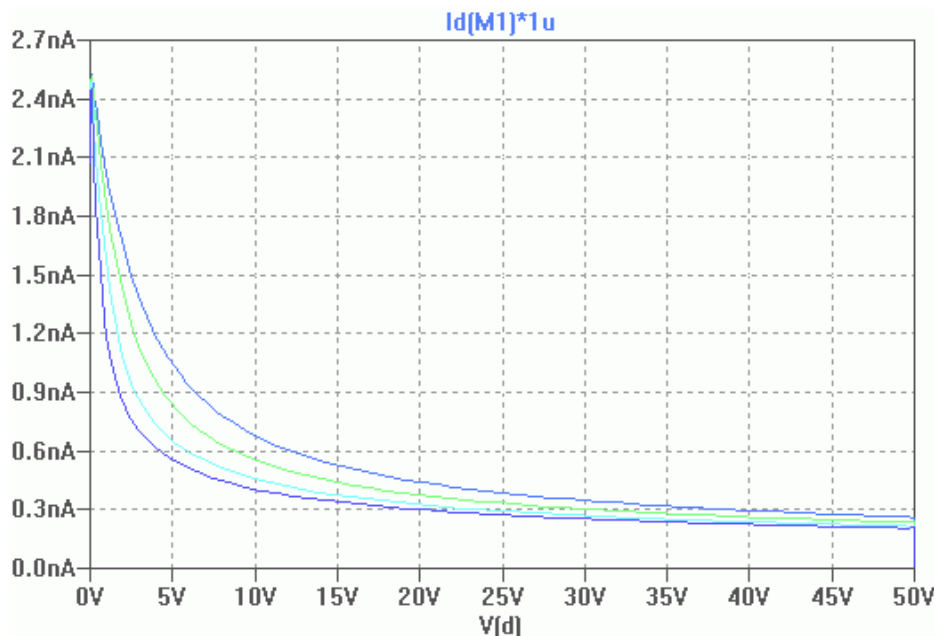
Illustration 9: IRFP240 MOSFET parameter 'a' stepped 0.3, 0.5, 1, 2

Probing Cds at Vds=10V is about right with **a=0.3**.

Parameter 'a' only affects the clipping region at high frequencies so is not important for audio amplifier simulations.

It would pay to go back and check the Gate charge to re-tweak Cgdmax and Cgdmin due to the new 'a' value above.

Tweaking gate resistor Rg

The gate resistor can be tweaked using the Rise time jig (download with the other jigs **Ref 11**).
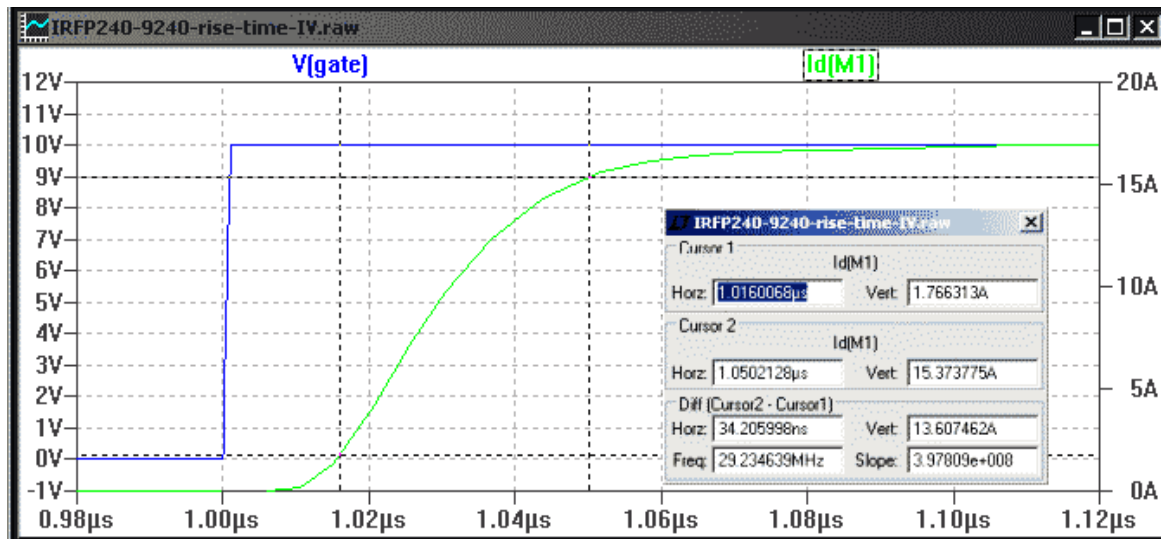
*Illustration 10: **IRFP9240 rise time jig with Rg of 9 ohms***

Set the gate voltage to the datasheet test circuit and the external gate and drain resistors to the values in the table that show the rise and fall times. For the IRFP9240 the typical rise time is 43ns with V_{DD} = - 100 V, I_D = - 11 A, R_{Gext} = 9.1 Ω, R_{Dext} = 8.6 Ω and a -10V input step. An Rg of 9 ohms gives 34ns rise time which is close enough for the IRFP9240. The Rg for the IRFP240 was chosen as 17 ohms (was 9 ohms from Hendrik's equation).

Summarising so far:

The new AC parameters in the -v5 model are below:

```
*VDMOS with subthreshold (c) Ian Hegglun fitted to 25C and 150C
.model IRFP240-v5 VDMOS (Rg=17 Vto=4.0 Vtotc=-5m Kp=6.5 Bex=-2.2 Lambda=4m
Rs=45m Rd=140m Ksubthres=0.1 Mtriode=0.3 Cgdmax=1.3n Cgdmin=10p a=0.3 Cgs=1.2n
Cjo=1n m=0.4 VJ=0.75 IS=25u N=1.5 Rb=19m Vds=200 Ron=0.18 Qg=45nC mfg=IHKT1907)
```

Tweaking the body diode DC parameters

Use the body diode jig for DC parameters [**Ref 11**]. These parameters are not significant for audio power amplifier simulations – they only affect reverse conduction if the SOA trips and audio SSR's. Body diodes models are important for resonant SMPS's.
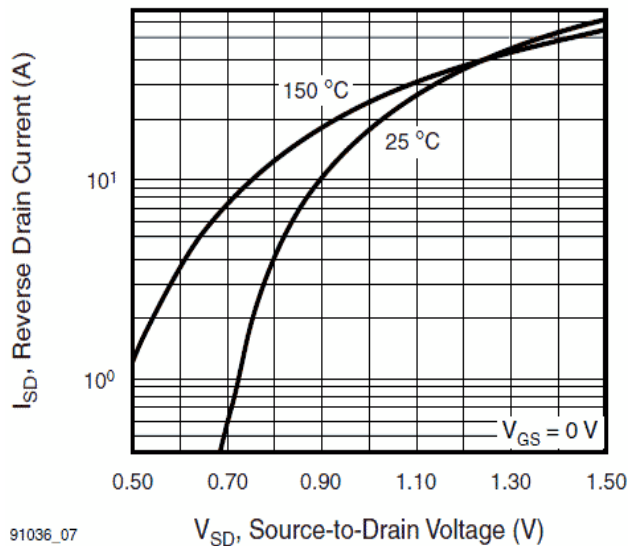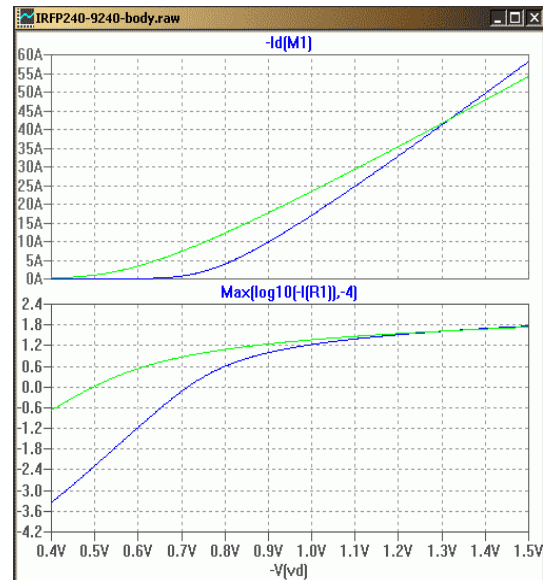
Illustration 11 IRFP240 body diode

Illustration 12 IRFP240 diode model

The first two parameters to fit are the diode saturation current parameter 'Is' and small Id slope 'N'.

Slope 'N' is extracted at 25°C. It has temp co parameters 'Eg' and 'Xti' for fitting the 150°C plot. With N=1 the slope is 60mV per decade of current at 25°C. The datasheet slope is about 1 decade per 100mV which means N is around 1.6. I chose **N=1.5** which is close enough.

The value of 'Is' was chosen by starting at 1pA and working up using the plot jig. Increasing 'Is' by a factor of 10 roughly doubles the current (Ln$_e$(10) = 2.3). Fit 'Is' using the low voltage end of the datasheet plot. The lowest for the IRFP240 datasheet is 0.7V for which Id is -0.6A for 25°C (diode current is technically negative for the n-channels since it is reverse drain current). **Is=10n** is OK.

Next choose Rb (body diode series resistance) for 25°C. This determines the high current region. If the current is too high then increase Rb. A quick starting value can be found (more easily than Hendrik's equation) by finding the rough change in current and change in voltage at the top end if the Id vs. Vd plot; for the IRFP240 datasheet at 25°C this is 10A for 0.1V, so try Rb ≈ 0.01 ohms.

This estimated Rb value was found to be about right using the plot jig. So it's **Rb=10m** at 25°C.

Next for 150°C two parameters are used: 'Trb1' for the high current end and 'Eg' for the low current end. 'Eg' is the band-Energy gap voltage which determines how temperature changes 'Is'. Parameter 'Eg' by default is 1.11V. In our example with N of 1.5 we can try 'Eg' = 1.5 for a starting value.

Eg=1.1 was found to a good fit for 150°C. Parameter Trb1=2.5m is chosen to get the crossing current to match the datasheet plot (crossing at 40A for the IRFP240).

Now we can list the new body diode parameters as the -v6 model below:

```
*VDMOS with subthreshold (c) Ian Hegglun fitted to 25C and 150C
.model IRFP240-v6 VDMOS (Rg=9 Vto=4.0 Vtotc=-5m Kp=6.5 Bex=-2.2 Lambda=4m Rs=45m
Rd=140m Ksubthres=0.1 Mtriode=0.3 Cgdmax=1.3n Cgdmin=10p a=0.3 Cgs=1.2n Cjo=1n
m=0.4 VJ=0.75 IS=10n N=1.5 Eg=1.1 Rb=10m Trb1=2.5m Vds=200 Ron=0.18 Qg=45nC
mfg=IHKT1907)
```

We are now done for the IRFP240 model. … The IRFP9240 is given below:

```
*VDMOS with subthreshold (c) Ian Hegglun fitted to 25C and 150C
.model IRFP9240h VDMOS (Nchan Rg=6 Vto=+3.76 Kp=9 Lambda=4m Rs=64m
Ksubthres=0.15 Mtriode=0.2 Rd=0.25  Rb=0.05 Bex=-2.3 Vtotc=-6m Tksubthres1=4m
Trs1=3.5m Trd1=5m Trb1=0 Cgdmax=1600p Cgdmin=30p a=0.5 Cgs=1400p Cjo=1000p m=0.4
Vj=0.75 N=7 Is=10u Eg=3.15 Vds=-200 Ron=0.5 Qg=44nC mfg=VishIH1907)
```

Notice the IRFP9240 requires a high 'N' value of 7. But in this case 'Eg' of 3.15 is not as high as 'N' like for n-channels. The IRFP9240 body diode plots are shown below:
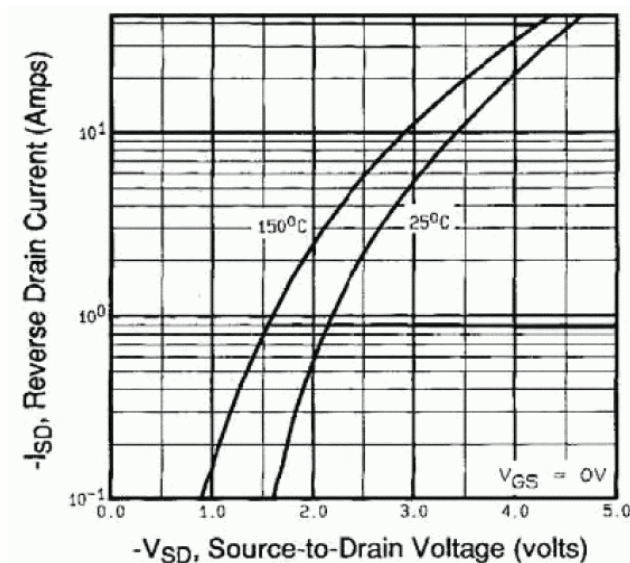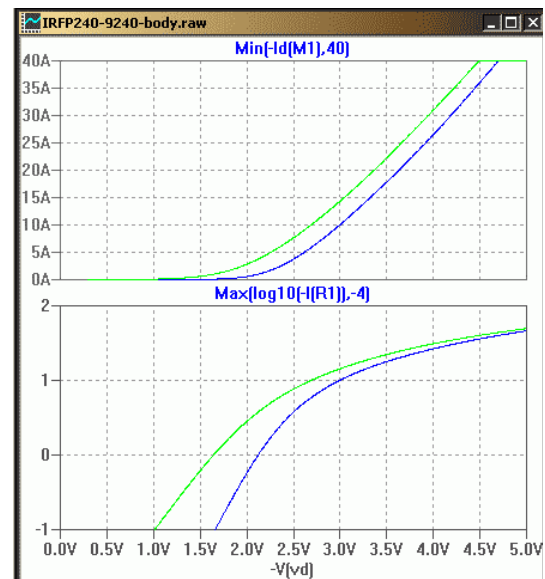

Illustration 13 IRFP9240 body diode

Illustration 14 IRFP9240 diode model

Summarising the finalised Quick model <u>after tweaking</u>:

The new AC parameters in the -v5 model are below:

```
*VDMOS with subthreshold (c) Ian Hegglun fitted to 25C and 150C
.model IRFP240-v6 VDMOS (Rg=17 Vto=4.0 Vtotc=-5m Kp=6.5 Bex=-2.2
Lambda=4m Rs=45m Rd=140m Ksubthres=0.1 Mtriode=0.3 Cgdmax=1.3n
Cgdmin=10p a=0.3 Cgs=1.2n Cjo=1n m=0.4 VJ=0.75 IS=10n N=1.5 Eg=1.1
Rb=10m Trb1=2.5m Vds=200 Ron=0.18 Qg=45nC mfg=IHKT1907)
```

------------------------ ----------------------

For an adventure! Using Graph grabber software to generate Tables for LTspice

Graph grabber software can be used to get many (x,y) points into a spreadsheet (Appendix 5). Then you can export the data in pairs for use in LTspice Table (...) function to generate both Id vs Vgs and Id vs Vds plots (Appendix 3).

Measured data for the RFP240 and IRFP9240 was imported into LTspice using Graph Grabber. The plots are shown below after the threshold voltages have been offset to match the Final models obtained from Vishay datasheets. Also the measured plots are scaled by a factor to get the curves to match the Final models. This assumes the Final models are the correct ones and the measured ones are different due to process variations or they are from a different source than Vishay.

The scale factor used for the two measured IRFP240's is 1.1 and the scale factor used for the two measured IRFP9240's is 1.3. This difference in Kp and gm is within the Max and Min range sometimes specified on datasheets. Those that have specified the Max and Min Gm values have about a ±variation from the typical value. The typical values are the ones we usually use for our models – unless we have enough samples (at least 10 per batch) over a long time frame (several years) to confidently use our measured means as the typical values.

Notice the p-ch measured data appears to show thermal runaway, possibly not fast enough sweeps with too high Vds. The n-channel drops at the top end and this can be caused when the drain voltage is not high enough to stay in the current saturation region (unlike the reference model which has adequate drain voltage).
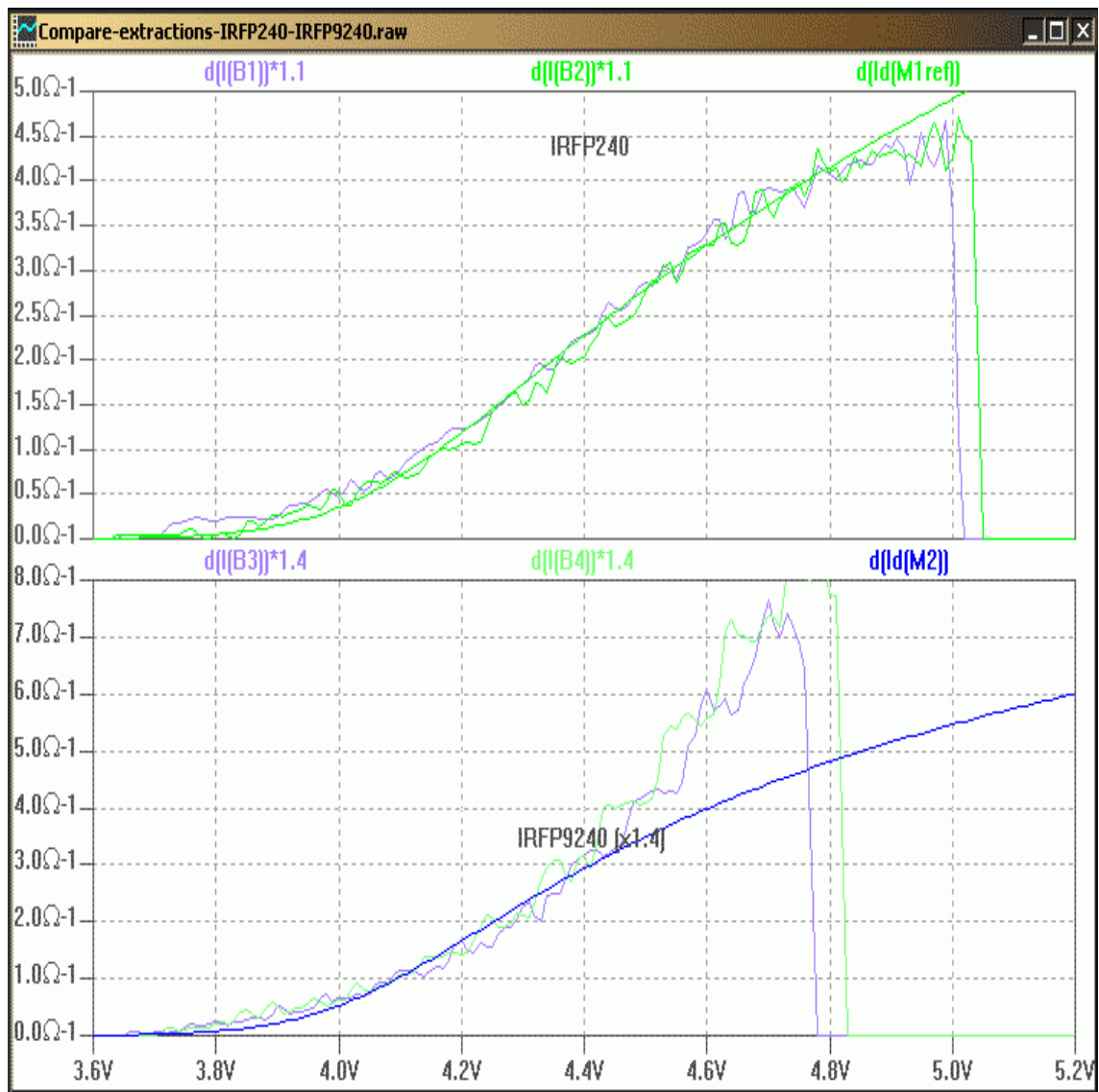
Illustration 15: Gm plots for measured IRFP240/9240 against our Final models

Summary

Hendrick's quick method gave quite good estimates for the VDMOS from the datasheets. They could be use without tweaking. But to get good capacitance and body diode parameters with temp co's some iterations are needed. And the plotter jigs are indispensable, making tweaking easy.

Once you have worked through this procedure it becomes quite easy. There is no need to import datasheet curves using Grap Grabber software – just a few key points from the datasheet plots are enough. The amount of time spent capturing the data, converting it and plotting it, does not get you that much more fitting accuracy and doubles the time to make a model.

Acknowledgements

20P20's samples to bench test for this report.

Thanks to Jan Didden of Linear Audio for taking a keen interest in my projects.

Thanks again to Steven Benbow for the free GraphGrabber software that can be downloaded here.

Last but not least Mike Engelhardt for making LTspice what it is, and for it's free use. Mike, thanks again for adding those temp co's to the VDMOS May 2019! They make the VDMOS much more accurate over temperature and easier to get then working as they should.

References

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2. Mike Engelhardt, 'Switcher CAD manual scad3', Feb 2010. Download. The Help file in the latest LTspice is usually fully up to date covering recent changes to the VDMOS etc.

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4. LTspice 'ChangeLog.txt' entry "12/16/14 Revised the subthreshold conduction equations for VDMOS." This file is located in the 'LTC' directory (with the program exe).

5. Bob Cordell, Book, 'Designing Audio Power Amplifiers', 2nd Edition includes new information on the VDMOS subthreshold parameter and more.

6. Francisco J. García-Sánchez; Adelmo Ortiz-Conde; et al, 'A unified look at the use of successive differentiation and integration in MOSFET model parameter extraction', J. Microelectronics Reliability, 2014. Available at Research Gate.

7. F. J. García-Sánchez; Adelmo Ortiz-Conde; et al, 'Revisiting MOSFET threshold voltage extraction methods', J. Microelectronics Reliability, 2012. Available at Research Gate. See Fig. 8, Fig. 9, they illustrate measurement 'noise' using the second derivative method.

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9. Dr Arto Kolinummi, 'Audio Power Amplifiers: Towards Inherently Linear Amplifiers', Linear Audio Press 2015, pp307. Ph.D Thesis at Tampere University of Technology, Finland, June 2010. https://linearaudio.net/books/2220

10. VDMOS models are posted at diyAudio.com here VDMOS models. Post #1 has fan-out links to the latest versions. Keantoken, thanks for maintaining this resource.

11. Several plotter jigs that are useful for tweaking parameters in this paper can be downloaded here https://paklaunchsite.jimdo.com/spice-models/

12. Hegglun, 'A subcircuit to add quasi-saturation to the VDMOS', June 2018, https://paklaunchsite.jimdo.com/spice-models/

13. Exicon datasheets http://www.exicon.info/PDFs/ECW20N20-Z.pdf http://www.exicon.info/PDFs/ECW20P20-Z.pdf

14. Kevin Aylward, SuperSPICE , https://www.anasoft.co.uk/download.htm includes the LTspice VDMOS model with quasi-saturation (since 2017).

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16. IRFP240 datasheet https://www.vishay.com/docs/91210/91210.pdf
IRFP9240 datasheet https://www.vishay.com/docs/91239/sihfp924.pdf
IRF640 datasheet http://www.vishay.com/docs/91036/sihf640.pdf

IRF9640 datasheet https://www.vishay.com/docs/91086/sihf9640.pdf

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Appendix 1. The LTspice jig for comparing two models

This jig plots two MOSFET's at once so you can see how close your model is to a reference model.

The reference model could be one obtained from the web as a subcircuit that is not in the VDMOS form and you want to convert it to the VDMOS form. To get a subcircuit to run you need to set the Prefix to letter 'X' (Ctrl+Rt click on the MOSFET symbol).

If you don't have a reference model then you could import data from a datasheet. But that takes a lot of time so you can just plot one MOSFET (Delete the unused plot or turn the other off in the plot window).

One very useful feature of this jig is the very easy way to switch from an (Id vs. Vgs) plot to an (Id vs. Vds) plot with only one change to the .dc card/lines (Step 2 below).

The jig can be downloaded from **Ref 11**. It comes with the IRFP240 and IRFP9240 models (as used for Part 1 of this paper).

Steps to use the jig
1. Open the file.

2. For Id vs Vgs
Choose the plot type (Top left corner)
1st card   `.dc V1 2 12 0.01`
2nd card   `;dc V2 0 30 0.01`   Note the semicolon is present.
Run
Edit `.Step param Vgs List 4 6 8` to set the Vgs plot range
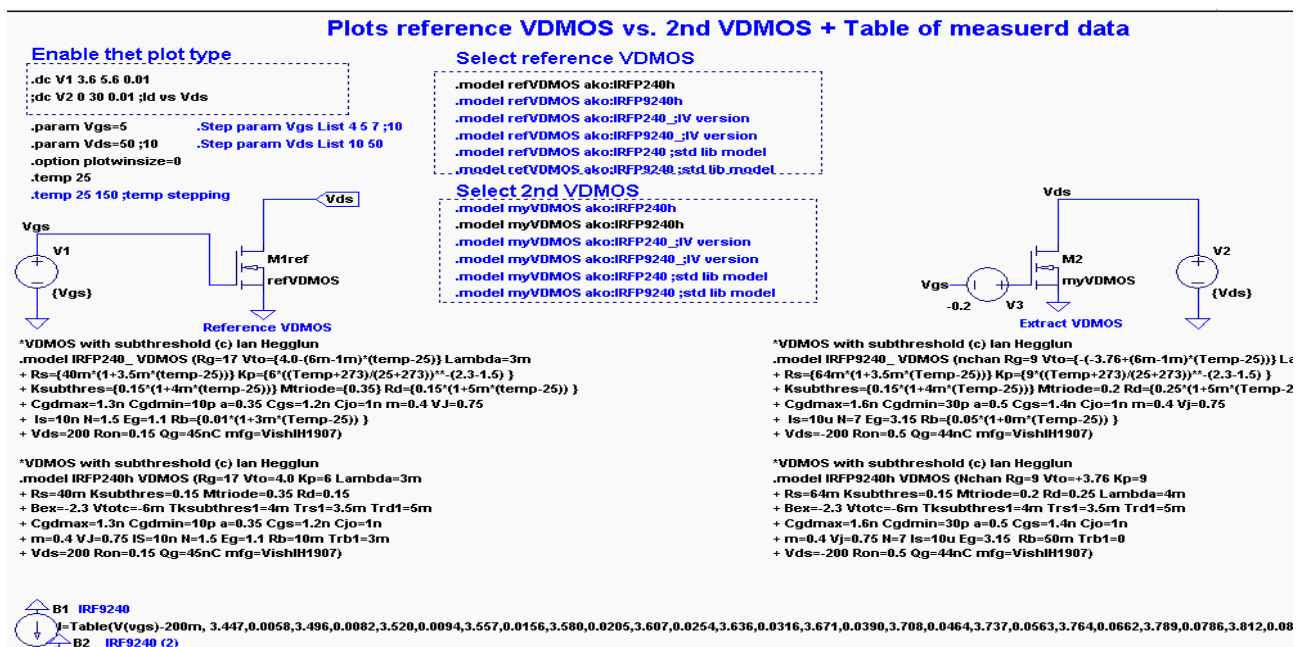Edit . `.param Vds=10` to set the Vds to match the datasheet (eg if you have Lambda>0)

Figure A1.1. The jig used to plot two VDMOS models for a comparison

3. For Id vs Vds
Choose the plot type (Top left corner)

1st card   `.dc V1 2 12 0.01`
2nd card   `.dc V2 0 30 0.01`   Edit out the semicolon and replace it with a full-stop.
Run. At the prompt choose the second card.
Edit `.Step param Vgs List 4 6 8` to set the Vgs plot range.

4. Select one reference VDMOS
Right click on the model you want and and select 'SPICE directive' button
Right click on the earlier model (in black) and and select 'Comment' button. Run

5. Select a 2nd VDMOS
Right click on the model you want and and select 'SPICE directive' button
Right click on the earlier model (in black) and and select 'Comment' button. Run

6. Plots can be turned off temporarily using eg I(B2)*0 and turning on again using I(B2)*1.
I(B1) plot is for Id vs Vgs plots from Table (…) data, and
I(B2) & I(B3) plots are for Id vs Vds plots from Table (…) data.

7. You can add other models. Other models can also be added as a test file using
`.include <Mymodel.txt>` to the jig (circuit). Place the text file `<Mymodel.txt>` in the same
directory as the jig files.

The plot below shows the IRFP240 and IRFP9240 VDMOS models compared to measured data.
The gm's are plotted here using the "d(Id...)" operator (first derivative if Id). Plotting Gm's gives
more useful information about how well the model represents the measured values, after all it is
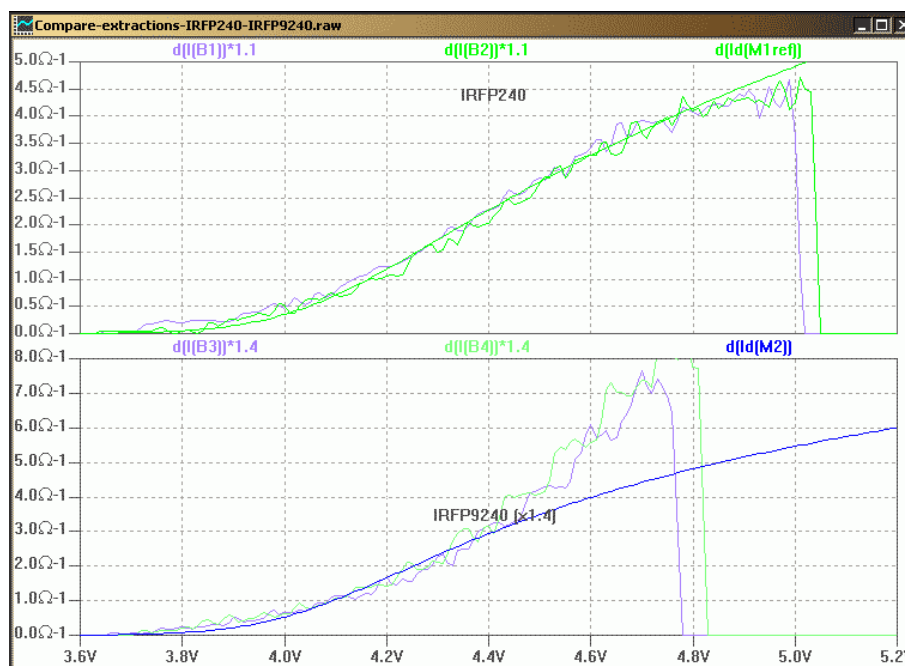Gm's (gain) and Id's that determine what distortion is generated in an amplifier.

Illustration 16: **Gm's for IRFP240 and IRFP9240 VDMOS models compared to measured data**

Note: The factors used for scaling in the above plots can't tell us much since in this case the data
provided did not include the temperature used not the Vds (since Vds can changes the effective Kp
value by up to 10% between using 50V or 5V).

Appendix 2.
Some equations for extracting Lambda and temp co parameters

1. Extracting Lambda (drain conductance parameter)

The Id versus Vds plots can give an idea of what value to use for Lambda in the VDMOS. Unfortunately, lateral power MOSFET's includes a quasi-saturation region up to a Vds of 20V as seen in **Figure A2.2** (near the end of the triode region) and this makes it hard to extract Lambda. At low Vds < 20V the slope is measurable so Lambda can be calculated, but for higher Vds >20V the slope is very close to zero.
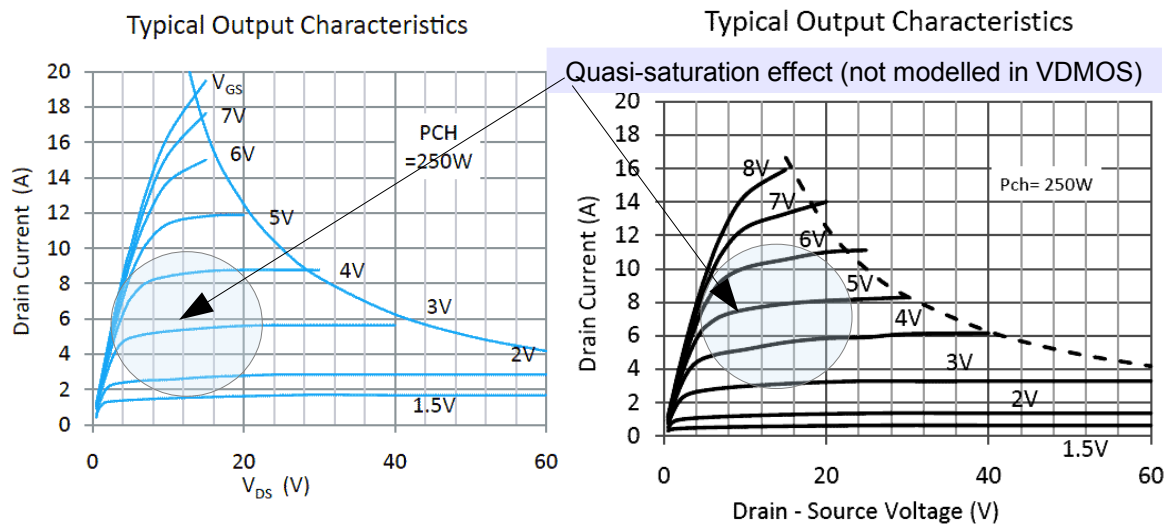

Figure A2.2. Output characteristic curves for Exicon ECW20N20-Z [L] and ECW20P20-Z [R]

One way is to take an average lope to cover the normal operating range of 10V to 100V (eg a 100W/8R amp). For example, using the N-ch Vgs=3V curve there is approximately ¼ A increase from Vds=10V to 60V which give Lambda=0.25A/50V or 5m[V^{-1}]. This is the value used. BTW A simple curve tracer that shows the quasi-saturation effect in the 'Hotter Spice' article [Ref 15].

2. Extracting the Bex Temperature Coefficient for Kp

For a wide temperature range we use the power-law 'Bex' (Beta exponent):

$$Kp_{Tj2} = Kp_{Tj1} \left(\frac{Tj2 + 273}{Tj1 + 273} \right)^{Bex}$$

where Bex is underlined negative and typically in the range of -1.5 to -2.5. The minus means Kp decreases with increasing temperature, and
where Tj1 is the lower temperature used on the datasheets, usually 25°C. The default temp for SPICE is 27°C so you need to add the statement `.Temp 25` to select the lower temperature for your model set up. To step two temperatures like 25°C and 150°C for datasheets then you can use use:

```
.Temp 25 50 .
```

An alternative temperature coefficient for Kp is J$_β$ and is calculated using:

$$Kp_{Tj2} = \frac{Kp_{Tj1}}{1 + J_\beta(Tj1 - Tj2)} \tag{1}$$

$$\text{so} \quad J_\beta = \frac{\left(\dfrac{Kp_{Tj2}}{Kp_{Tj1}} - 1\right)}{Tj2 - Tj1} \tag{2}$$

But this formula is not suitable for very low Tj2 (when Tj2<<Tj1) since the denominator can go to zero. For wide temperature range high <u>and</u> low we use the power-law form with exponent Bex.

To converting from J_β to Bex it was found that a J_β of 9m/C requires a Bex of -2.5 and a J_β of zero requires a Bex of zero. So the scale factor for is Bex is -2.5/9m = -273 times (add the minus).

$$Bex \approx -273 \cdot J_\beta$$

3. The threshold voltage temperature coefficient (VtoTc)
The threshold voltage temperature coefficient VtoTc is used to calculate Vth at a different temperature to Tref:

$$Vth_{T2} = Vto - VtoTc(T2 - Tref) \tag{3}$$

Where Vto is the threshold voltage at the reference temperature Tref (default is 27°C and datsheets is 25°C)

Choosing the threshold voltage temperature coefficient using the 'ztc' point

In amplifier simulations we sometimes want the zero temperature coefficient point to be accurate. The ZTC voltage and current can be found from pulse tests or ball park figures from datasheets.

The ZTC point is where the drain current does not alter with changes in junction temperature. It is the result of the rise in drain current from the threshold voltage falling with Tj increasing being cancelled by the fall in Kp (and fall in gm at a particular current) with Tj increasing. Since $Id_{ztc}(Vgs)$ is independent of temperature it is possible to find solve for Tcv once we have found Kp's temperature coefficient using:

$$Id_{Tref} = \frac{Kp_{Tref}(Vgs_{internal} - Vto)^2}{1 + J_\beta(Tref - Tref)} = Id_{T2} = \frac{Kp_{Tref}(Vgs_{internal} - [Vto - VtoTc(T2 - Tref)])^2}{1 + J_\beta(T2 - Tref)}$$

Therefore a helpful initial threshold temperature coefficient is:

$$VtoTc \approx \frac{J_\beta}{2}(Vgs_{ztc} - Vto) \tag{4}$$

where J_β is the temperature coefficient of Kp and the factor of ½ comes from approximating 1-$\sqrt{(1+x)} \approx \frac{1}{2}x$). We also neglect small differences in Vto's due to Rs. This gives an approximate temperature coefficient. BTW the gm versus Vgs ztc point occurs at a different Vgs to the Id versus Vgs ztc point so don't mistake it for the Id ZTC point.
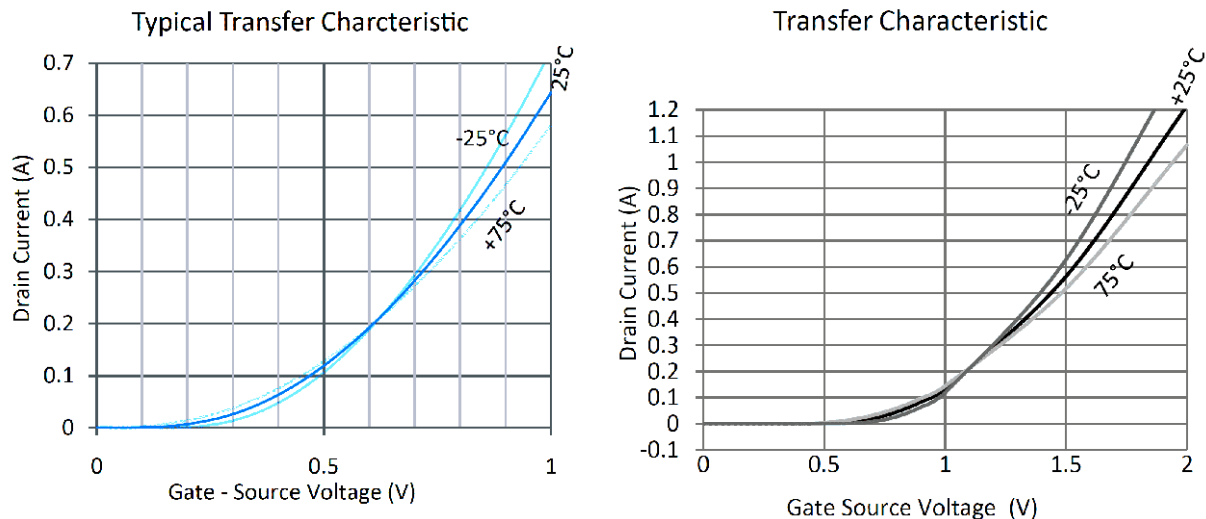
Figure A2.1. Right datasheet Exicon ECW20N20-Z at low Id. Left 20P20 [Ref 13].

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Appendix 3.How to export points from spreadsheet to LTspice Table(...)

Step 1: Set up a new sheet to collate selected points ready for exporting to text file

In a new sheet use equations to get selected (x,y) points ready for exporting to text file. You can get away with plotting in Vgs increments of 100mV for the first 1V above the threshold voltage and then 0.5V steps which requires 30 pairs to cover a 10V Vgs range. Use the equation "=Sheet1:A3" to get the value of cell A3 on Sheet1 into the destination cell in say Sheet2. You do do this using the mouse by typing equals in the destination cell of Sheet2 then click on Sheet1 tab and click on cell A3 and press Enter – you are now in sheet 2 with "=Sheet1:A3" automatically entered into the destination cell. Repeat for the other value of the pair. Select the 2 destination cells and drag down and you will see all the other values from Sheet1 in Sheet2. Then remove unwanted ones. In OpenOffice use "Shift+minus>Enter" to delete a row where the cursor is placed (or several selected rows) more quickly.

You can export several different groups at once by adding more groups under the first group. For example Vgs,Id for 25°C as the first group, and Vgs,Id for 75°C for the second group, Vgs,gm for 25°C as the third group, and Vgs,gm for 75°C as the third group. If you want to include other values such as for the complement FET then add them more groups. If you want to also include datasheet values then add them more groups. Putting all of them on one sheet reduces the amount of post editing next for of the exported text file. In OpenOffice to export first save your spreadsheet, then use SaveAs>csv>remove the " text delimiter and leave blank>OK, then Close the file. Rename the csv file as a txt file.

In the next section you edit the OpenOffice values exported as a "csv" (comma separated values) file (which is a plain text file where each rows is exported as a line with comma separators ending with a return).

Step 2: Open the csv file (renamed as a txt file) using OpenOffice Writer and accept the default import character set (Western Europe ASCII US).

For use in LTspice all values need to be in a long string as pairs x1,y1,x2,y2,... with no returns. Use Search/Replace to remove the returns and substitute commas. In OpenOffice use $ as the Search character for a return, and as the Replace character use a comma. You also need to tick Regular Expressions "More Options" box to recognise the $ as special expression. Then click Replace All, then Save the file. Select the data points and Copy/Paste into an LTspice

Table(V(Vin),<paste-here>).

How to smooth out glitches in datasheet curves

Some datasheets show a step change in current which can be caused by changing ranges on a meter or changing current sensing resistors. The 2012 ALFET datasheet curves have glitches at Vgs=4V as seen in Figure A3.1. This glitch in current can be removed in LTspice using a correction factor of 1.023 with an equation scaling the Table() function using equation

```
I=If(U(V(Vin)-4),1.023,1)*Table(V(Vin)+50m,0,.0001,...)
```

Vin has 50mV added to offset the datasheets curves so they appear on to of the measured curves. This is valid since ALFET threshold voltages vary by +/-50mV from device-to-device (d-MOSFETs can vary by +/-200mV). ALFET Kp is fairly constant between devices of the same polarity (maybe +/-5 percent) and across batches to within maybe +/-10 percent.

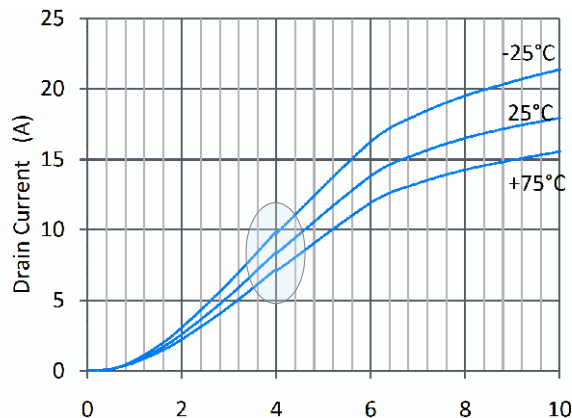**Figure A3.1. Original Datasheet curves with 'glitch' at Vgs=4V**

Tip: The gm's in Figure 7 are plotted using d(Id). The gm's of the measured data are plotted using Table(...) values as I(B5)/V(1v) and I(B6)/V(1v). Division by 'V(1v)' is a trick to plot currents as gm's to get units A/V to match d(Id) units of A/V (shown as Ω-1 in LTspice plots).

Appendix 4 is moved to the end of Part 2

Appendix 5. Using a GraphGrabber software

GraphGrabber can be downloaded here by Steven Benbow. Thanks Steve! The steps are:

1. If a PDF is supplied zoom to 400% and use the Snapshot Tool and drag over the graph. Alternative: use PrtScrn. Save the clipboard to a gif or jpg.

2. Open GraphGrabber then open the graphic file: File>Open image

3. Zoom out/in so the plot fills the working area, then use Crop to restrict the view to just the plot plus a margin

4. Click 'Set X-axis' and drag a line from the peak to the RHS edge, then enter the X values (refer to your original PDF). If you want logarithm scale click 'Log' (just visible under the Max) then 'OK' (to be certain, check it, Right Click on "X-axis" and mouse over 'Change Scale Type' shows which it is, and can change it to 'Log' if not Log).

5. Click 'Set Y-axis' and drag a line from the peak to the bottom edge, then enter the Y values (lesser value then higher value) in this case the higher is –40 and the lesser needs to be calculated from the indicated values.

6. Before adding a data series zoom in say 200% so the curve extends past the screen (you can use the sliders later to move it while capturing points).

7. Click 'Add Data Series' and I started on the LHS at the curve start. I used 100mV increments over

8V gate voltage range and this is adequate for calculating the derivative in a spreadsheet (needed to plot d√Id versus Vgs).

8. Click 'To End Data Series'. Then File>Export Graph As Data File (default is CSV).

9. Open a spreadsheet eg OpenOffice or Excel.

10. Open the CSV file and copy the data list to the clipboard. Paste the data into the spreadsheet. Alternative: Open the .csv file using the spreadsheet File>Open.

11. Select the data and add a X-Y scatter graph.

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Appendix 6. New LT-IV temp models compatible with new VDMOS Temp Co's

My earlier 'Tja' and 'Tjp' VDMOS models have been replaced using the new Temp Co's (May 2019). These models only work in LT-XVII (or later).

I continue to use LT-IV due to older PC's. I use a new alternate models that run in LT-IV but uses the new LT-XVII VDMOS parameters. They use curly bracket equations that are backward compatible with the same parameters as the new LT-XVII VDMOS model parameters.

Those continuing with LT-IV can use my new alternate VDMOS model parameters that were extracted for the new model. Also these alternative models will run in LT-XVII without any editing of the models (they are just more cumbersome with those curly bracket equations).

The earlier '.param Tja=<val> and .param Tjp=<val> statements can still be used but in a different way – you now assign Tjp=<val> after each MOSFET name you want to make different temperatures to the other parts – all others are by default at the global 'ambient' temperature.

The following curly bracket equations are used for Vto, Kp, Rs, Ksubthres, Rd, and Rb as seen in the new alternative model for LT-IV below:

```
*VDMOS with subthreshold (c) Ian Hegglun
.model IRFP240_ VDMOS (Rg=5 Vto={4.0-(6m-1m)*(Temp-25)} Lambda=3m
+ Rs={40m*(1+3.5m*(Temp-25))} Kp={6*((Temp+273)/(25+273))**-(2.3-1.5) }
+ Ksubthres={0.15*(1+4m*(temp-25))} Mtriode=0.35 Rd={0.15*(1+5m*(Temp-25)) }
+ Cgdmax=1.3n Cgdmin=10p a=0.35 Cgs=1.2n Cjo=1n m=0.4 VJ=0.75
+ Is=10n N=1.5 Eg=1.1 Rb={0.01*(1+2.5m*(Temp-25)) }
+ Vds=200 Ron=0.15 Qg=45nC mfg=VishIH1907)
```

The corresponding new LT-XVII model is:

```
*VDMOS with subthreshold (c) Ian Hegglun
.model IRFP240h VDMOS (Rg=5 Vto=4.0 Kp=6 Lambda=3m
+ Rs=40m Ksubthres=0.15 Mtriode=0.35 Rd=0.15
+ Bex=-2.3 Vtotc=-6m Tksubthres1=4m Trs1=3.5m Trd1=5m
+ Cgdmax=1.3n Cgdmin=10p a=0.35 Cgs=1.2n Cjo=1n
+ m=0.4 VJ=0.75 IS=10n N=1.5 Eg=1.1 Rb=10m Trb1=2.5m
+ Vds=200 Ron=0.15 Qg=45nC mfg=VishIH1907)
```

Xti by default is 3. The default is used, so Xti is not specified in most VDMOS models.

On the the new alternative model for LT-IV

Parameter 'Eg' is the temp co for the body diode 'Is' and curly bracket equations are not needed for 'Is' since 'Eg' is a parameter in the old VDMOS. The value of 'Eg' can be copied across unchanged from the new VDMOS model to the alternative model for LT-IV, likewise 'Is' is copied across.

VtoTc and Bex are inserted into the curly bracket equations below (highlighted values):

```
Vto={4.0-(6m-1m)*(Temp-25)}
Kp={6*((Temp+273)/(25+273))**-(2.3-1.5)}
```

These values come from the new VDMOS model and are offset by the internal temp co parameters in the old VDMOS (that are carried across to the new LT-XVII as defaults). This means the alternative model for LT-IV above will also operate perfectly in LT-XVII as well with no changes. The curly bracket equations do the offsetting so you don't need to do any calculations (which may introduce an error ☺) and be careful to preserve the brackets around these internal offsets.

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Appendix 7. The VDMOS parameter Mtriode

A useful undocumented parameter in the VDMOS is the 'Mtriode' parameter which scales the voltage where the MOSFET enters/leaves saturation such as for hard clipping allowing a good model fit for lateral MOSFET's with typically less than 1% average error over a wide current range which is very good for the compact equations used in VDMOS model.

Mtriode is be applied to the ohmic region equation and the saturation region is not affected by Mtriode. The equation is:

$$Id_{triode} = Kp(1 + Lambda\ Vds)\frac{W}{L}\left(Mtriode(Vgs - Vto) - Mtriode^2\frac{Vds}{2}\right)Vds$$

The equation was RE'd using a jig (available for download ref 11). The following steps are below:

Zwerver: Linear Region: Vds<Vgs-Vth

$$Id = Kp\frac{W}{L}(1 + \lambda \cdot Vds)\left(Vgs - Vto - \frac{Vds}{2}\right)Vds$$

Set Lambda=0 for now. When Vds = Vgs – Vto

$$Id_{sat} = \frac{Kp}{2}Vds^2$$

for Vto=4, Vgs=5 Kp=1 then Id-sat=0.5A

$$G_D = \frac{d\ Id}{d\ Vds} = Kp(Vgs - Vto) - Vds$$

for Vto=4, Vgs=5 Kp=1 then G_D ramps down from 1A/V to 0.

Mtriode scales G_D initial slope and Vds for the end of the triode region

$$G_D(Mtriode) = \frac{d\ Id}{d\ Vds} = Kp(Vgs - Vto) \cdot Mtriode - Vds * ?$$

(reality check Vto=4, Vgs=5 Kp=1 Vds=0 Mtriode=0.5 then G_D = 0.5A/V ← agrees with jig)

Now Vds ends the triode region when G_D = 0 so the previous "?"

$$\times(Vds - sat) = Kp \cdot Mtriode(Vgs - Vto)$$

for Vto=4, Vgs=5 Kp=1 Vds=0 Mtriode=0.5 then we want Vds-sat to be 2V so the "?" factor must be Mtriode^2, giving

$$G_D(Mtriode) = Kp(Vgs - Vto)Mtriode - Vds \cdot Mtriode^2$$

To get back to the original equation integrate G_D after rearranging

$$G_D(Mtriode) = Kp \cdot Mtriode[(Vgs - Vto) - Vds \cdot Mtriode]$$

integrating gives

$$Id_{triode} = Kp\ Mtriode\frac{W}{L}(1 + \lambda \cdot Vds)\left(Vgs - Vto - Mtriode\frac{Vds}{2}\right)Vds$$

use I(B1) to generates the current for the above equation and plot d(I(B1)) with MOSFET d(Id(M1)).

The equation in a behavioural source gives the same as the VDMOS model when Mtriode is changed to whatever. It agrees! So the formula above is correct for Mtriode.

Equation for solving for Mtriode from a point near pinchoff

Choose a point before saturation on the Id,Vds plot.

$$Mtriode = \frac{Vgs - Vto}{Vds} - \sqrt{\frac{(Vgs - Vto)^2}{Vds^2} - \frac{2\,IpX}{Kp\,(1 + Lambda \times Vds)\,Vds^2}}$$

When Kp has been extracted from saturation don't use Lambda (ie Lambda=0 for this equation) because it is already part of the Kp. But do use Lambda in the final VDMOS parameters, where Lambda can be solved using the equation:

$$Lambda = \frac{1}{IdY\,(VgsY - VdsY)/(IdY - IdX) - VgsY}$$

Where IdX,VdsX and IdY,VdsY,VgsY are 2 points from the Id(Vds) curve at a chosen Vgs. These two points need to be in saturation, eg X just after pinchoff and Y a far right point. Lambda is the inverse of the Early voltage V_A, and V_A is the x-axis intercept of the tangent from saturation.

**Figure A7.1. [L] Point M for calculating Mtriode (just before pinchoff)
[R] Points X and Y for calculating Lambda (just after pinchoff and the RHS)**

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… <mark>There is also a Part 2 available</mark>: PakLaunchSite.jimdo.com/spice-models/ mirrored at Ian'sGoogleDrive